FPGA-based Modelling of Aging Effects and Implementation of IP-Cores for Wear-Out-Detection

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***Abstract*— The paper will give some background information on a SEU-TID IP-Core for monitoring of single events and aging effects especially for flash-based FPGAs using floating gate transistors. The concept was verified by real measurements in medical radiation environments. A new special implementation IP of a ring oscillator is used to show the asymmetrical degradation for TID sensitivity and charge loss of transistors. It was simulated with a real-number modelling methodology (VHDL-RNM). This special implementation is also applicable for ASICs and SRAM-FPGA technologies. In addition a new IP architecture was developed to also detect aging effects due to normal wear-out mechanisms like electrical and thermal stress and charge trapping of transistors and floating gates, e.g. due to NBTI or HCI. The results of accelerated life and stress tests will be discussed.**

Keywords*— *CMOS, FPGA, Radiation, Total Ionizing Dose, TID, Single event upsets, SEU, Real Number Modeling, RNM, Ring Oscillator, ROSC, Aging, Wear-Out, Process Control Modules, PCM, RedunSys, RADSAGA

I. INTRODUCTION

In ionizing radiation environments there are basically two effects on electronics [1][2][3]: Single event effects (SEE) like transients/upsets (SET/SEU) and Total ionizing dose (TID).

Single events or soft errors can lead to loss of functionality depending on FIT (Failure in Time) rate and system complexity, e.g. bitflips in configuration memories like SRAM in FPGA or any other configuration Flipflops. Whereas TID is an accumulated effect which results in performance degradation depending on dose rate and time, e.g. threshold shifts in transistors and increase in delay time and leakage current.

In the research project RedunSys [4] a first version of monitoring circuit for these effects with flash-based FPGAs from Actel/Microsemi [5][6] in ProAsic3 technology (130nm) was designed. Soft errors could not be detected because of low test times and system complexity. Therefore the focus was towards TID measurement. The results are shown in Figure 1. There is a linear degradation of the frequency of the ring oscillator during the first 400Gy (40krad) and an exponential degradation with higher dose rate. Also a kind of annealing is seen afterwards. After a dose rate above ~1000Gy (100krad) some devices stopped operation due to hardware defects.

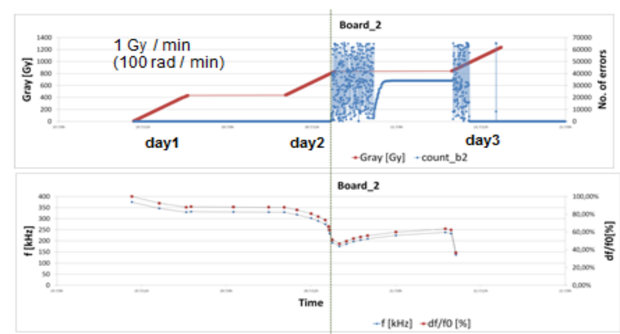

Figure 1: Measurement results in medical radiation environments

In the meantime some work on the topic was done by Kastensmidt [8], Berg [9]], Wang [16] and it was observed that the floating gate (FG) transistor in flash-based FPGAs is the main contributor for TID effects in this kind of FPGAs[7]. Especially charge trapping in oxide and STI (shallow trench isolation) regions of the transistors can cause voltage shifts and parasitic leakage current (Michalowska-Forsyth [10], Schlenvogtm [11]).

After some further studies post RedunSys a detailed analysis of the behavior in more detail with VHDL-RNM (real number modelling) was done [12]. An optimized SEU-TID core was developed. The basic results are discussed in next section II.

Finally the radiation based aging concept was applied to classic aging, e.g. through electrical and thermal stress [13]. This is shown in chapter III.

The IP-core was redesigned for stress measurements to perform accelerated aging with several test setups and measurements. The concept is shown in section IV with the measurements shown in section V. In section VI and VII the findings are summarized and future plans are discussed.

II. BACKGROUND

A. SEU-TID IPcore

The principle architecture of the optimized IP core [14] is shown in Figure 2. The new features introduced are

- Fault insertion
- JTAG/TCL interface
- Temperature independent aging Index (%)
- Encrypted VHDL (configuration by VHDL generics)

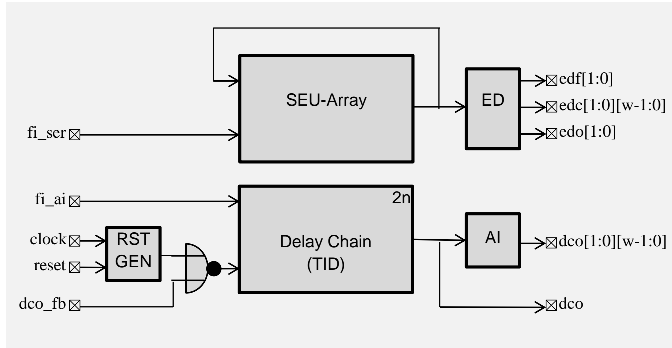

Figure 2: Architecture of SEU-TID IP-Core

B. Flash-based FPGA Technologies

In the older Microsemi FPGA technologies like ProAsic3/SmartFusion (130nm), IGLOO2/SmartFusion2 (65nm) the radiation sensitive FG transistor, which is basically used for configuration programming, is also located in the datapath of basic versatiles (LUTs). Thus, it is sensitive to performance degradation regarding delay and leakage current. Therefore some safety margins are included in the models and libraries [7][15]. Our measurement results in the RedunSys projects shown in Figure 1 are within these limits regarding delay and dose rate.

In the newer Microsemi technologies like RTG4 (65nm) and Polarfire (28nm) the FG transistor is decoupled from the data path to eliminate its TID sensitivity for delay degradation [16].

C. TID effects and transfer curve

In Figure 3 the transfer curve of a CMOS inverter is shown. Due to TID over time the threshold voltages are modified resulting in a shift of the switching level to the left and slope modification due to resistive changes. Also voltage degradation at both levels may be infected due to leakage current. All these effects contribute to parameter, delay, leakage and performance degradation of the transistors and gates sensitive to TID.

D. VHDL-RNM of FG in datapath

In Figure 4 a basic data path of an OR2 gate is shown. It consists of several inverters, a path gate MUX and some FG pass transistors in series. This example was modelled according the transfer curve definitions with VHDL-RNM (real number modeling), a kind of switch level modelling and simulation style of RC topologies using a digital VHDL simulator.

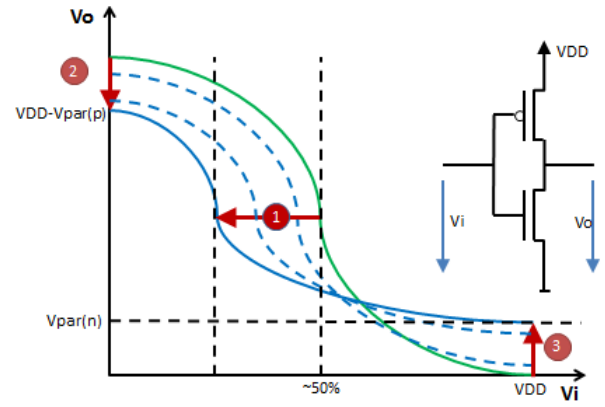

Figure 3: TID & Transfer Curve

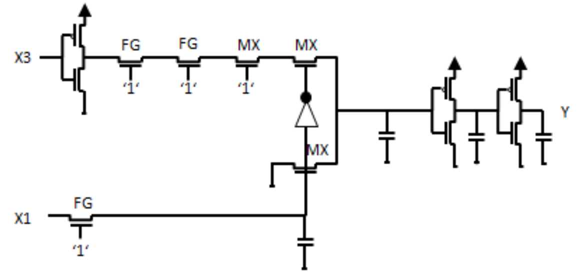

Figure 4: VersaTile: Y=X1 or X3

```vhdl
entity rosc_2nor2_rnm is
    generic (
        g_VDD   : real := 1.2;       -- core VDD [V]
        g_L     : real := 130.0e-9; -- gate length [m]
        g_Wpmos : real := 780.0e-9; -- gate width p [m]
        g_Wnmos : real := 390.0e-9; -- gate width n [m]
        g_proc  : real := 10000.0;  -- process factor
        g_n2pmob: real := 2.0;       -- p to n mobility
        g_swl   : real := 0.50;      -- switch level %
        g_Cint  : real := 40.0e-15; -- internal cap [F]
        g_dt    : real := 0.01e-9;  -- sampling periode [sec]
        -- radiation factors
        g_rfswl : real := 0.0;  -- switching level % (transfer curve)
        g_rfRp  : real := 0.0;  -- resistor p % (delay, slope)
        g_rfRn  : real := 0.0;  -- resistor n % (delay, slope)
        g_rfRfg : real := 0.0;  -- Resistor FG % (delay, slope)
        g_rfVdp : real := 0.0;  -- voltage degradiation p % (leakage i)
        g_rfVdn : real := 0.0;  -- voltage degradiation n % (leakage i)
        -- toplevel
        g_lrosc : integer:= 10;      -- length of ROSC (2 cells per stage)
        g_reset : time    := 100 ns -- init/reset);
end entity rosc_2nor2_rnm;
```

Figure 5: NOR2_RNM (Generics, with radiation factors)

All the parameters shown in Figure 5 were adjusted and refined accordingly to the simulation results of the first real radiation measurements done within the RedunSys project in 2010.

E. Simulation results without FG transistors

We also modelled and simulated simpler ROSC structures without FG transistors (e.g. Microsemi's RTG4 technology) to look for any degradation of the characteristic frequency of the implemented ROSC. We compared with results from Microsemi [16] and also found no measureable degradation. This is shown in Table 1.

700 inverters, 65um, normal		[ns]	TID10/TID0	r/f
TID0% (Vth=0.6V)	rising edge	228,200	n.a.	100,31%
	falling edge	227,500		
TID10% (DeltaVth=+-0.06V)	rising edge	229,956	100,77%	100,16%
	falling edge	229,592	100,92%	

Table 1: Simulation results without FG

F. Special Implementation of ROSC-IP

After some more detailed investigations, simulation and mathematics a special ROSC was implemented. The results of these simulations are shown in Table 2

700 inverters, 65um, special		[ns]	TID10/TID0	r/f
TID0% (Vth=0.6V)	rising edge	126,700	n.a.	100,84%
	falling edge	125,650		
TID10% (DeltaVth=+-0.06V)	rising edge	138,250	109,12%	119,70%
	falling edge	115,500	91,92%	

Table 2: Simulation results with special ROSC-IP

The simulation results now show degradation of delay in the same order of percentage like the variance of the applied radiation factors for threshold shifts and resistive degradation. This was proven only by Mathematics (Figure 6) & RNM-Simulations and not by real measurements yet. The assumption is that asymmetrical TID effects are masked by the nature of normal ring oscillators (inverted feedback loop). We are still in close cooperation and discussions with the RADSAGA@Cern research project [17] for further explanations and applications of the IP.

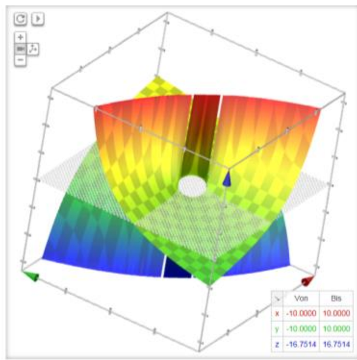

Figure 6: Principle Mathematics of ROSC-IP

III. Classic Aging & Wearout

In several discussions based on the TID background above we were asked from various sites to check whether our TID monitoring concept for radiation based aging can also be applied to classic aging. According [18][19][20] these effects basically are:

- Electrical stress
- Thermal stress
- Mechanical stress
- Electromigration
- Negative-bias temperature instability (NBTI)
- Hot-carrier injection (HCI)
- Tunnel Effect

IV. DUT & Stress Concept

We redesigned the TID-IP-core for stress testing and implemented various architectures for stress, biasing and duty cycle modifications. The DUTs were several SMF2000 SmartFusion2 SoC FPGA Modules [21] (Figure 7) from Trenz Electronic (12 kLUT). We implemented the following features:

- INV-chain with 10000 inverters
- Internal frequency measurement (100MHz clock)
- Sequencer for functional mode and test mode
- Timer for cascaded measurement

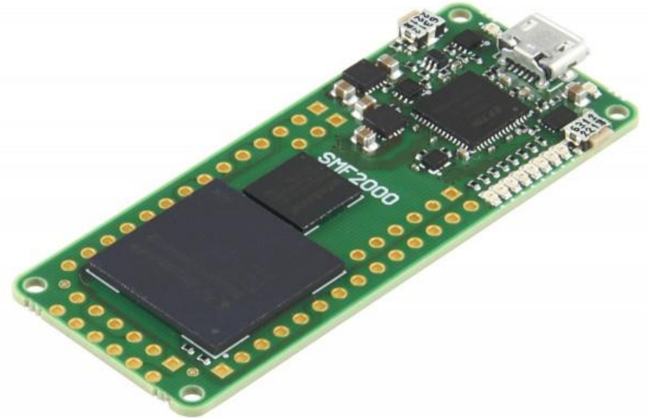

Figure 7: SMF2000

Four different stress architectures were implemented with different stress levels:

1) BIAS: static during functional mode
2) ROSC: ring oscillator mode
3) STRESS: 400MHz stress-frequency
4) STRESSMAX: 400MHz, Vcore=1.5V (default:1.2V)

V. Measurements

A. Test Setup1

In one test setup four devices were measured at a time. This was done by an implementation of a sequencer to perform cascaded measurements with stress cycling of around 9 min stress time and 3 min ROSC measurement. The original characteristic frequencies are shown in Table 3.

Board#	Architecture	F0/kHz
#0	STRESS	182
#2	BIAS	193
#7	STRESSMAX	250
#5	ROSC	193

Table 3: Setup1

In Figure 8 the four frequencies can be seen. Each measurement cycle is about 3min. The STRESSMAX shows an increase of the frequency depending of the temperature annealing after each stress period.

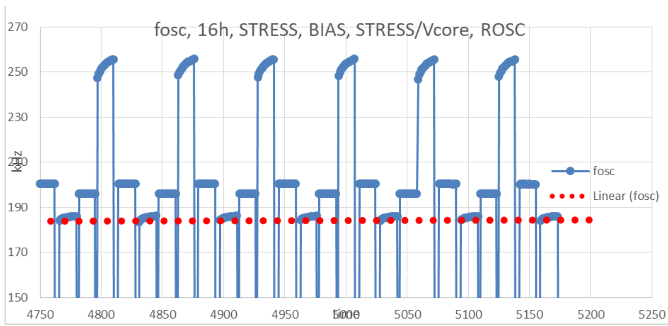

Figure 8: Cascaded f-measurement details

The temperature behavior of STRESSMAX and STRESS is shown in Figure 9 and in more detail in Figure 10. The delta temperature with regards to room temperature of ~24°C is about 48°C vs. 31°C which corresponds to the increased power dissipation (~50%).

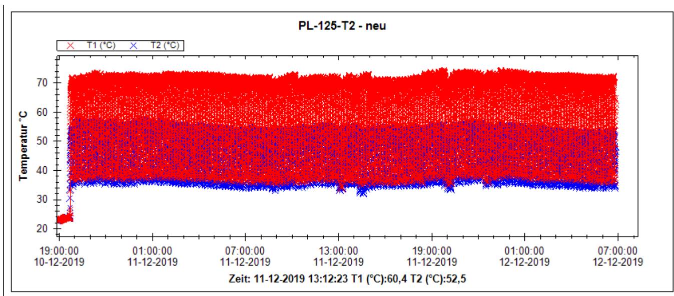

Figure 9: Stress test 400 MHz, 1.2V (blue), 1.5V(red)

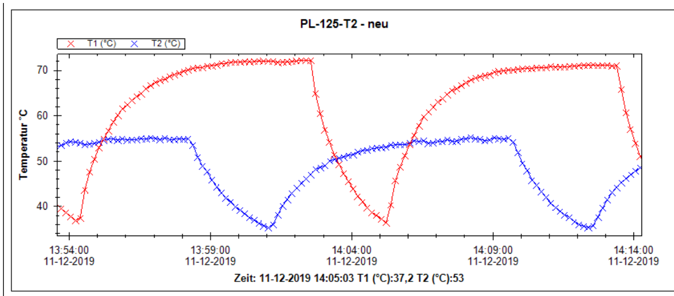

Figure 10: Stress test 400 MHz, Temperature details

Board#	Architecture	F0/kHz	F0/kHz 16h	delta f %	delta T/ns
#10	BIAS	206	206	0,0%	0
#3	ROSC	195	196	0,5%	-26
#6	STRESS	205	200	-2,5%	122
#4	STRESSMAX	266	256	-3,9%	147

Table 4: Setup2, Results after 16h

The frequency over the whole 16h measurement period is shown in the net spiral of Figure 11. A small degradation of about 5 kHz (-2%) can be seen at the end of the test.

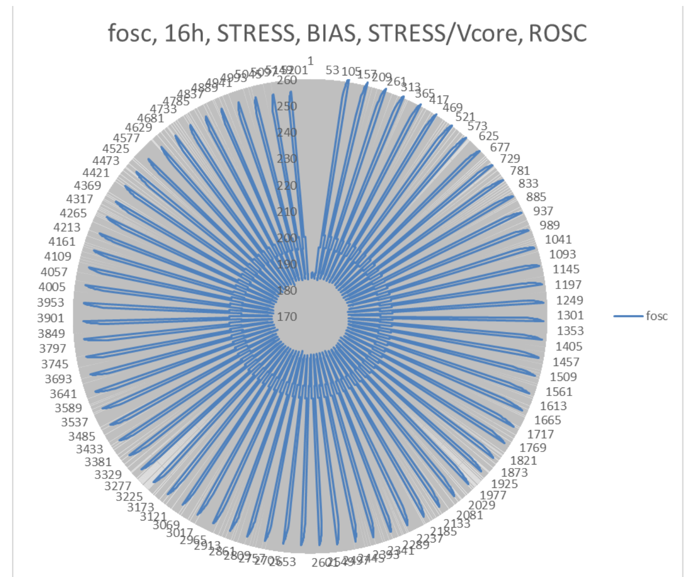

Figure 11: Cascaded f-measurement, 16h test

B. Test Setup2

In a more detailed test with Setup2 and measurement after 16 hours we saw a deviation of about 2.5% for STRESS and 3.9% for STRESSMAX (Table 4).

VI. Discussion of Results

A clear trend can be seen in above results. But the absolute values has to be taken with care because the delay of the inverters depend on the process, voltage and junction temperature (PVT). Especially the internal core voltage could not be tracked thus voltage drops or ripple and offset on the external voltage regulator due to their degradation (temperature, power) could not be determined. The same is true for the internal temperature which may also vary e.g. due to hotspots.

The stress duty cycle was chosen for enabling a kind of continuous measurements during the test time. Thus annealing between the stress periods may also have some unreliable effects. Therefore further tests with continuous stress or increased duty cycle periods are in preparation.

The internal frequency measurement depend on the system frequency which is generated internally by PLL and oscillators. They may also be degraded internally or due to the external voltage regulators. Thus an external frequency measurement and analysis is strongly recommended.

VII. Conclusion & Further Work

Discussions with RADSAGA@Cern are ongoing concerning the ROSC-IP which could be of interest for all semiconductor vendors and CMOS technologies (PCM, Monitoring IP etc.).

It has been shown that it is in principle possible to use the TID monitoring concept also for classic aging and wear-out measurements. Some results still have to be repeated and analyzed in more detail and the demonstrator has to be refined accordingly. The investigation of other FPGA technologies like Microsemi Polarfire or Xilinx FPGAs depending on customer requests, requirements and priorities are in discussion.

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